

PRELIMINARY

CY62148

Features

- 4.5V–5.5V operation
- · CMOS for optimum speed/power
- Low active power
- 660 mW (max.) • Low standby power (L version)
 - —2.75 mW (max.)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE options

Functional Description

The CY62148 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}), an active LOW output enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 99% when deselected.

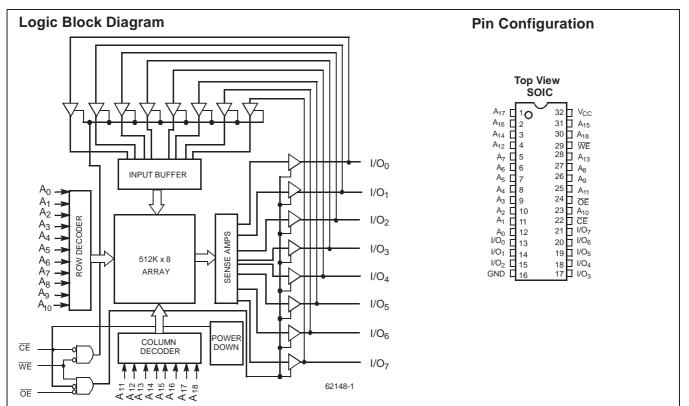
512K x 8 Static RAM

Writing to the device is accomplished by taking chip enable one (\overline{CE}) and write enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₈).

Reading from the device is accomplished by taking chip enable one (\overline{CE}) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}) . Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY62148 is available in a standard 450-mil-wide body width SOIC package.



Selection Guide

| | | | CY62148-55 | CY62148-70 |
|------------------------------|------------|------------|------------|------------|
| Maximum Access Time (ns) | | | 55 | 70 |
| Maximum Operating Current | Commercial | | 120 mA | 120 mA |
| Maximum CMOS Standby Current | Commercial | Commercial | | 2 mA |
| | | L | 0.5 mA | 0.5 mA |

Shaded areas contain advance information



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Maximum Ratings

| (Above which the useful life may be impaired. For user guide-lines, not tested.) |
|---|
| Storage Temperature65°C to +150°C |
| Ambient Temperature with Power Applied55°C to +125°C |
| Supply Voltage on V_{CC} to Relative GND ^[1] –0.5V to +7.0V |
| DC Voltage Applied to Outputs in High Z State $^{[1]}$ 0.5V to $\rm V_{CC}$ +0.5V |

Electrical Characteristics Over the Operating Range^[3]

| DC Input Voltage ^[1] | –0.5V to V _{CC} +0.5V |
|---------------------------------|--------------------------------|
| Current into Outputs (LOW) | 20 mA |

Operating Range

| Range | Ambient Temperature ^[2] | V _{CC} |
|------------|---------------------------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | –40°C to +85°C | 5V ± 10% |

| | | | | | 621 | 48–55 | 621 | 48–70 | |
|------------------|--|--|--------------------------|------|------|----------|------|--------------------------|----------|
| Parameter | Description | Test Conditions | | Min. | Max. | Min. | Max. | Unit | |
| V _{OH} | Output HIGH Voltage | $V_{CC} = Min., I_{OH} = -1 mA$ | | | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 2.1 mA | | | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | | | | | 2.2 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage ^[1] | | | | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I _{IX} | Input Load Current | $GND \le V_I \le V_{CC}$ | $GND \le V_I \le V_{CC}$ | | | +1 | -1 | +1 | μA |
| I _{OZ} | Output Leakage Current | $GND \le V_I \le V_{CC}$, Output I | Disabled | | -5 | +5 | -5 | +5 | μA |
| I _{CC} | V _{CC} Operating Supply Current | $V_{CC} = Max.$ $I_{OUT} = 0 mÅ,$ $f = f_{MAX} = 1/t_{RC}$ | Com'l | | | 120 | | 120 | mA |
| I _{SB1} | Automatic CE Power-Down Current —TTL Inputs | $\begin{array}{l} \text{Max. } V_{CC}, \ \overline{CE} \geq V_{IH} \\ V_{IN} \geq V_{IH} \ \text{or} \\ V_{IN} \leq V_{IL}, \ f = f_{MAX} \end{array}$ | Com'l | | | 15 | | 15 | mA |
| I _{SB2} | Automatic CE Power-Down Current —CMOS Inputs | $\label{eq:max_vcc} \begin{array}{l} Max. \ V_{CC}, \\ \overline{CE} \geq V_{CC} - 0.3V, \\ V_{IN} \geq V_{CC} - 0.3V, \\ \text{or } V_{IN} \leq 0.3V, \ \text{f=0} \end{array}$ | Com'l | L | | 2 500 | | 2 500 | mA μA |

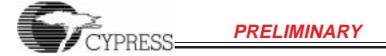
Shaded areas contain advance information

Capacitance^[5]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|---|------|------|
| C _{IN} | Input Capacitance | $T_A = 25^{\circ}C, f = 1 \text{ MHz},$ | 10 | pF |
| C _{OUT} | Output Capacitance | $V_{CC} = 5.0V$ | 10 | pF |

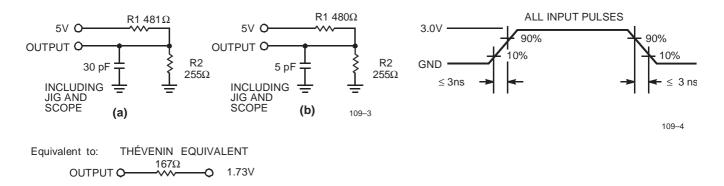
Notes:

V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
T_A is the "instant on" case temperature.
See the last page of this specification for Group A subgroup testing information.
Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
Tested initially and after any design or process changes that may affect these parameters.



CY62148

AC Test Loads and Waveforms



Switching Characteristics^[3,6] Over the Operating Range

| | | 6214 | 48–55 | 6214 | 8–70 | |
|-------------------|-------------------------------------|------|-------|------|------|------|
| Parameter | Description | Min. | Max. | Min. | Max. | Unit |
| READ CYCLE | | | • | • | | |
| t _{RC} | Read Cycle Time | 55 | | 70 | | ns |
| t _{AA} | Address to Data Valid | | 55 | | 70 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | ns |
| t _{ACE} | CE LOW to Data Valid | | 55 | | 70 | ns |
| t _{DOE} | OE LOW to Data Valid | | 20 | | 35 | ns |
| t _{LZOE} | OE LOW to Low Z | 0 | | 0 | | ns |
| t _{HZOE} | OE HIGH to High Z ^[7, 8] | | 20 | | 25 | ns |
| t _{LZCE} | CE LOW to Low Z ^[8] | 3 | | 3 | | ns |
| t _{HZCE} | CE HIGH to High Z ^[7, 8] | | 20 | | 25 | ns |
| t _{PU} | CE LOW to Power-Up | 0 | | 0 | | ns |
| t _{PD} | CE HIGH to Power-Down | | 55 | | 70 | ns |
| WRITE CYCLE | [9] | • | | | | |
| t _{WC} | Write Cycle Time | 55 | | 70 | | ns |
| t _{SCE} | CE LOW to Write End | 45 | | 60 | | ns |
| t _{AW} | Address Set-Up to Write End | 45 | | 60 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | ns |
| t _{PWE} | WE Pulse Width | 45 | | 50 | | ns |
| t _{SD} | Data Set-Up to Write End | 45 | | 55 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t _{LZWE} | WE HIGH to Low Z ^[8] | 3 | | 3 | | ns |
| t _{HZWE} | WE LOW to High Z ^[7,8] | | 20 | | 25 | ns |

Shaded areas contain advance information.

Notes

Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified 6. I_{OL}/I_{OH} and 100pF load capacitance.

t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage. 7.

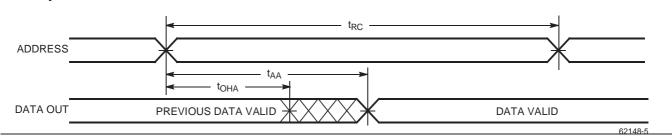
8.

At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZCE} , and t_{HZWE} is less than t_{LZWE} is less than 9.

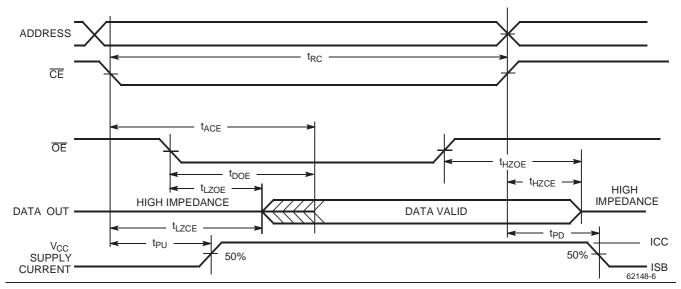


Switching Waveforms

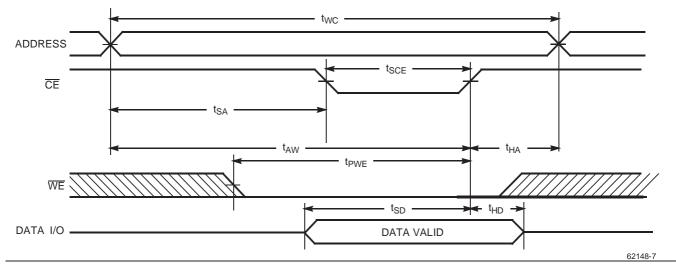
Read Cycle No.1^[10,11]



Read Cycle No. 2 (OE Controlled)^[11,12]



Write Cycle No. 1 (CE Controlled)^[13,14]



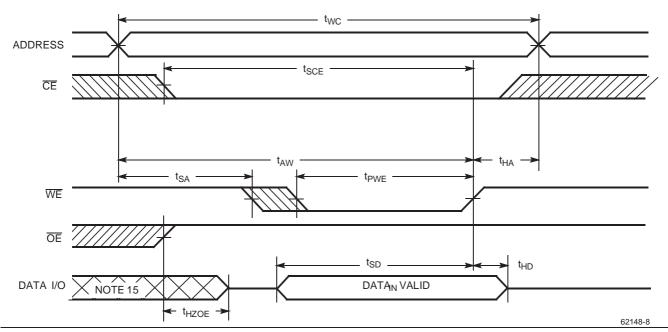
Notes:

Device is continuously selected. OE, CE = V_{IL}.
WE is HIGH for read cycle.
Address valid prior to or coincident with CE transition LOW.
Data I/O is high impedance if OE = V_{IH}.
If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

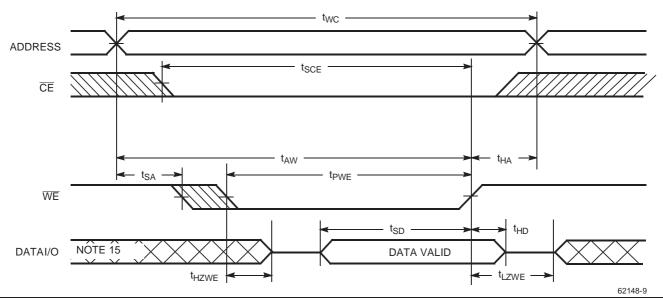


Switching Waveforms (continued)

Write Cycle No. 2 (WE Controlled, OE HIGH During Write)^[13,14]



Write Cycle No.3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[13,14]



Note:

15. During this period the I/Os are in the output state and input signals should not be applied



Truth Table

| CE ₁ | OE | WE | 1/0 ₀ – 1/0 ₇ | Mode | Power |
|-----------------|----|----|-------------------------------------|----------------------------|----------------------------|
| Н | Х | Х | High Z | Power-Down | Standby (I _{SB}) |
| Х | Х | Х | High Z | Power-Down | Standby (I _{SB}) |
| L | L | Н | Data Out | Read | Active (I _{CC}) |
| L | Х | L | Data In | Write | Active (I _{CC}) |
| L | Н | Н | High Z | Selected, Outputs Disabled | Active (I _{CC}) |

Data Retention Characteristics Over the Operating Range

| Parameter | Description | Conditions | Min. | Max | Unit |
|-------------------|--------------------------------------|--|-----------------|-----|------|
| V _{DR} | V _{CC} for Data Retention | No input may exceed V_{CC} + 0.5V | 2.0 | | V |
| I _{CCDR} | Data Retention Current | $\begin{array}{l} V_{CC} = V_{DR} = 2.0V, \\ \overline{CE} \geq V_{CC} - 0.3V \\ V_{IN} \geq V_{CC} - 0.3V \text{ or } V_{IN} \leq 0.3V \end{array}$ | (Com'l) | 200 | μΑ |
| | | $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$ | (Ind'l) | 500 | μΑ |
| | | | (Mil) | 2 | mA |
| t _{CDR} | Chip Deselect to Data Retention Time | | 0 | | ns |
| t _R | Operation Recovery Time | | t _{RC} | | ns |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---------------|---------------|-----------------|-------------------------------|--------------------|
| 55 | CY62148-55SC | S34 | 32-Lead (450-Mil) Molded SOIC | Commercial |
| 55 | CY62148L-55SC | S34 | 32-Lead (450-Mil) Molded SOIC | Commercial |
| 70 | CY62148-70SC | S34 | 32-Lead (450-Mil) Molded SOIC | Commercial |
| 70 | CY62148L-70SC | S34 | 32-Lead (450-Mil) Molded SOIC | Commercial |
| 70 | CY62148-70SI | S34 | 32-Lead (450-Mil) Molded SOIC | Industrial |
| 70 | CY62148L-70SI | S34 | 32-Lead (450-Mil) Molded SOIC | Industrial |

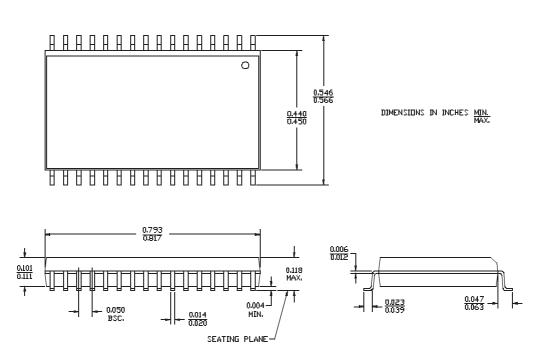
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Package Diagrams



32-Lead (450 Mil) Molded SOIC S34